EE 505

Lecture 13

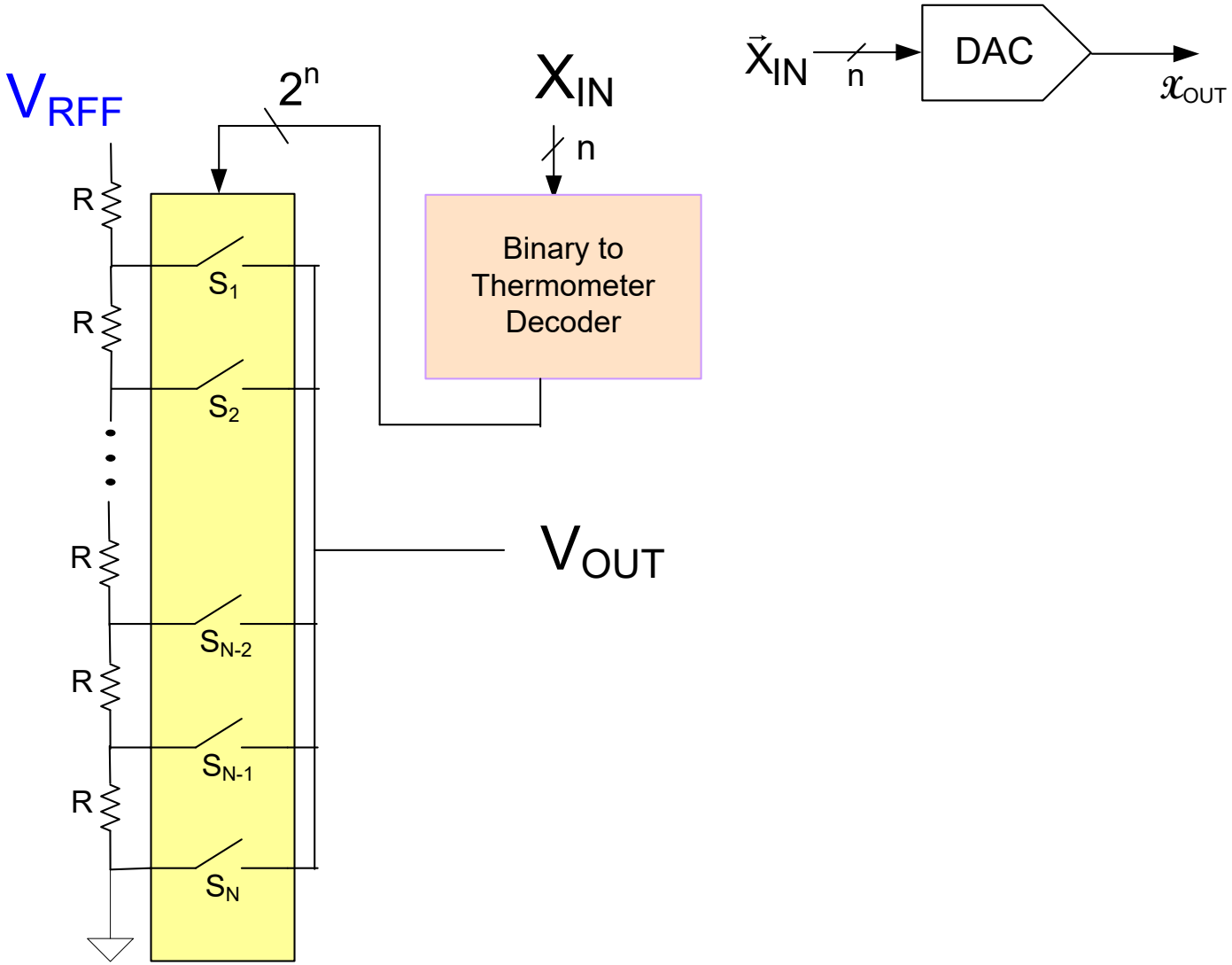
String DACs

Current Steering DACs

Review from Last Lecture

DAC Architectures

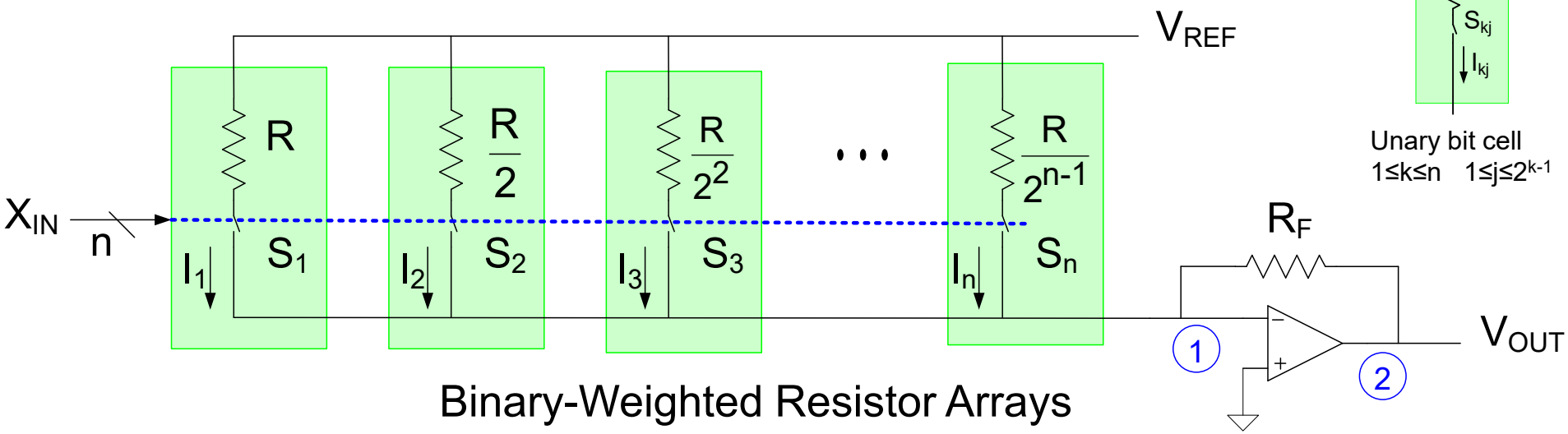
R-String



Basic R-String DAC including Logic to Control Switches

DAC Architectures

Current Steering



Binary-Weighted Resistor Arrays

- Unary bit cells usually bundled to make resistors
- Same number of unary cells needed as for thermometer coded structure
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

Review from Last Lecture

DAC Architectures

Charge Redistribution

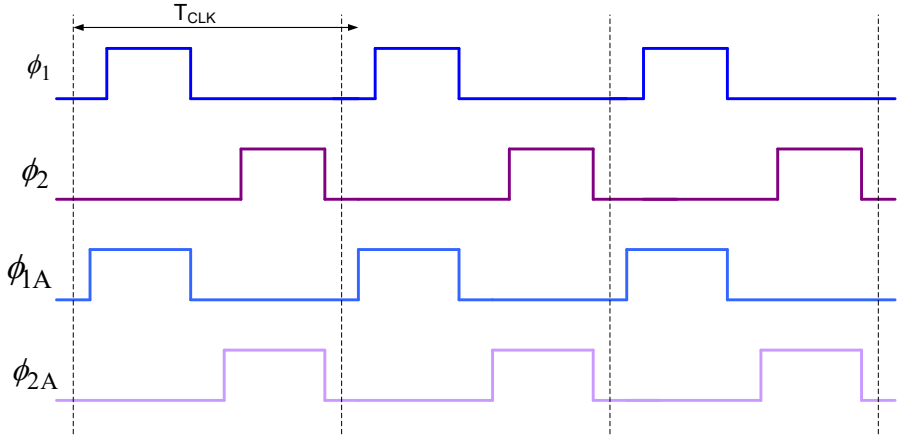
$$Q_{SET} = V_{REF}\sum_{i=0}^{n-1} d_i C 2^i$$

$$Q_{RDIS} = V_{OUT}\, 2^n C$$

$$Q_{SET} = Q_{RDIS}$$

$$V_{REF}\sum_{i=0}^{n-1} d_i C 2^i = V_{OUT}\, 2^n C$$

$$V_{OUT} = V_{REF}\sum_{i=0}^{n-1} d_i 2^{i-n}$$

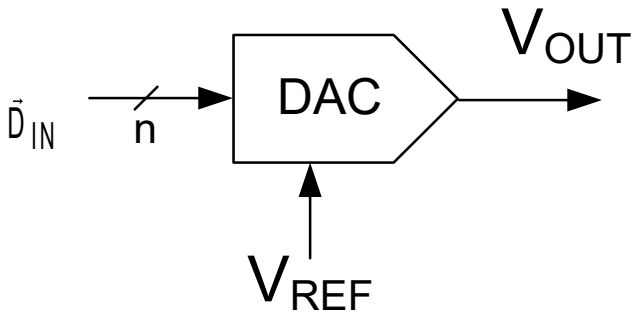


Note capacitor values play no role in this analysis, only capacitor ratios

Review from Last Lecture

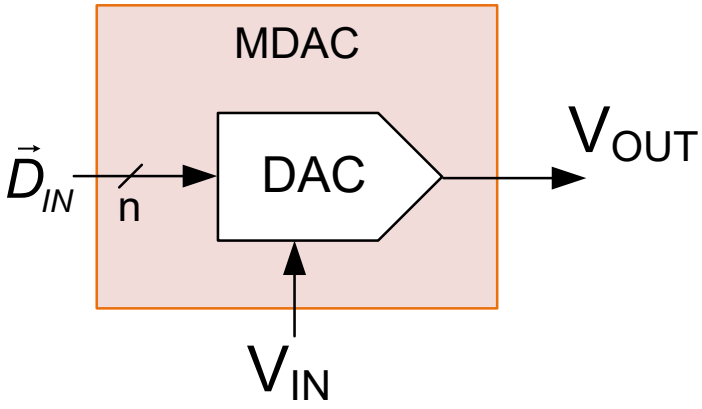
DAC Architectures

MDAC (Multiplying DAC)



V_{REF} fixed or limited range

$$V_{OUT} = V_{REF} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$



V_{IN} Variable, often positive or negative

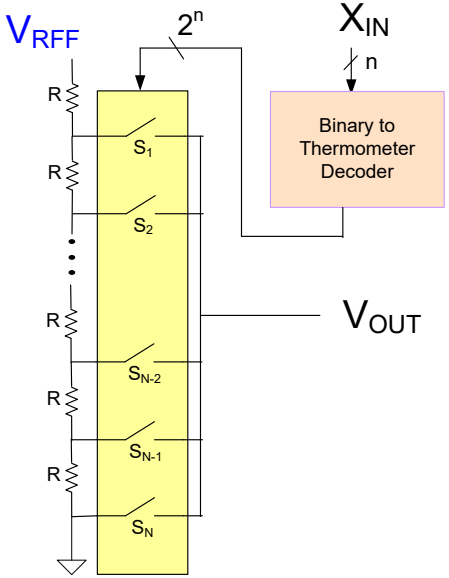
$$V_{OUT} = V_{IN} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$

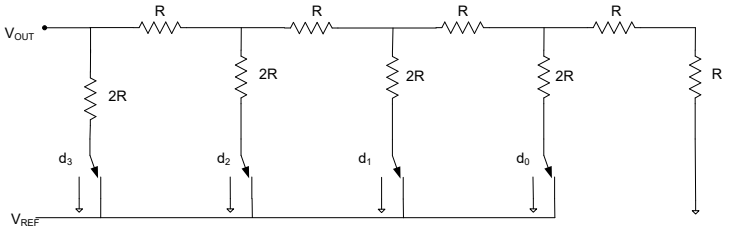
- Some define MDACs to be DAC structures that have current outputs
- Many DAC structures can perform well as a MDAC (possibly one quadrant)
- Performance of some DAC structures limited if V_{REF} is varied

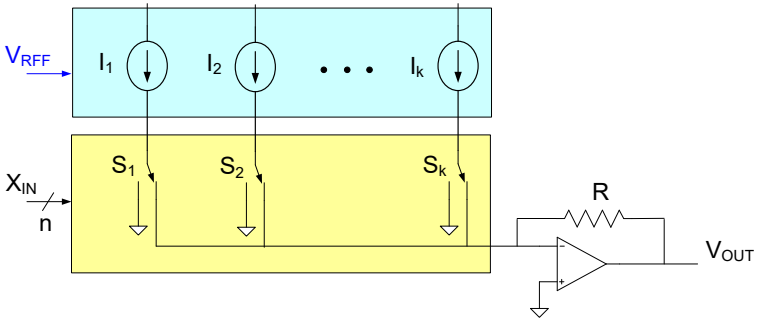
Review from Last Lecture

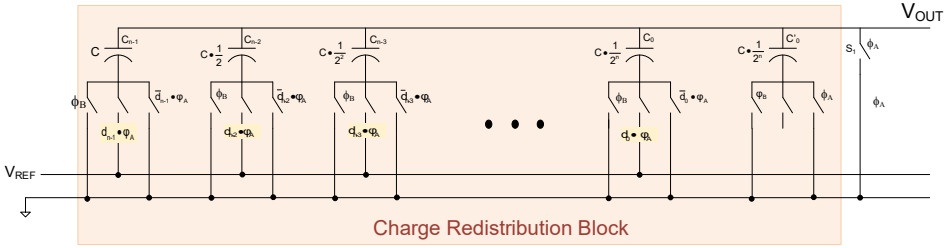
DAC Architectures

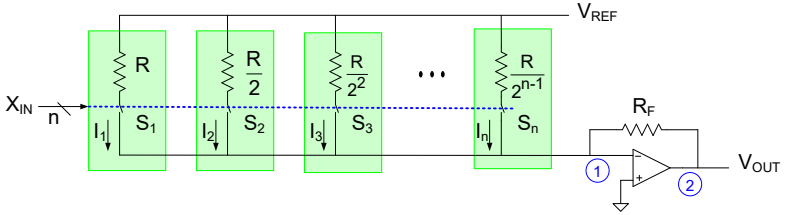
Suitable as MDAC?





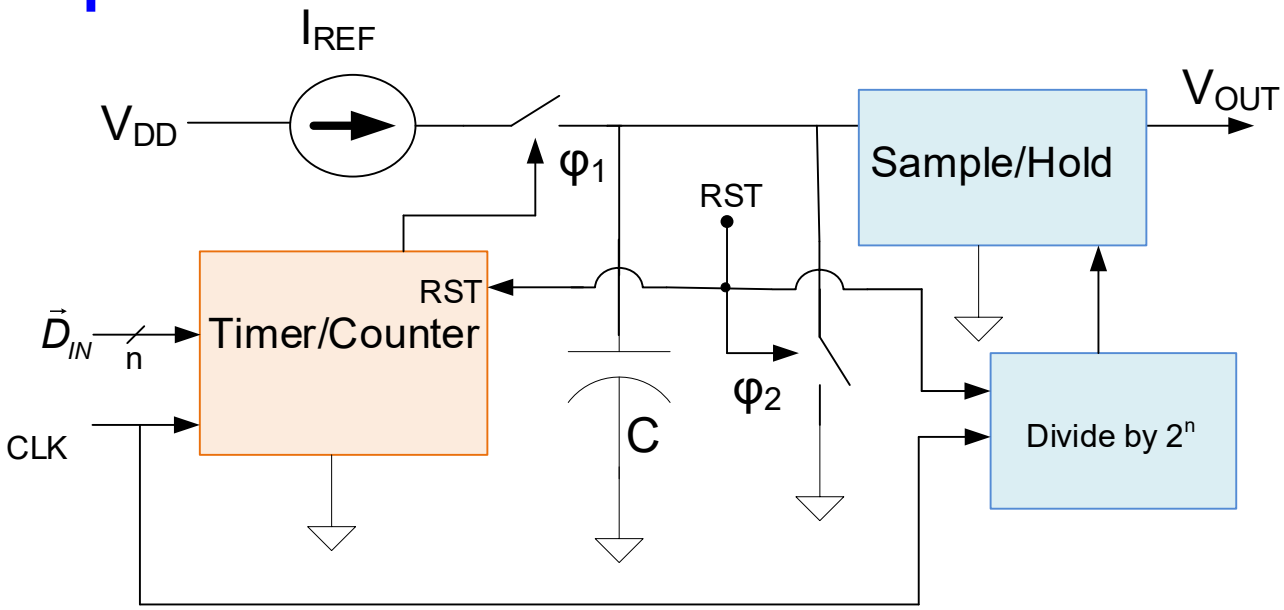






DAC Architectures

Single Slope



Single-Slope DAC

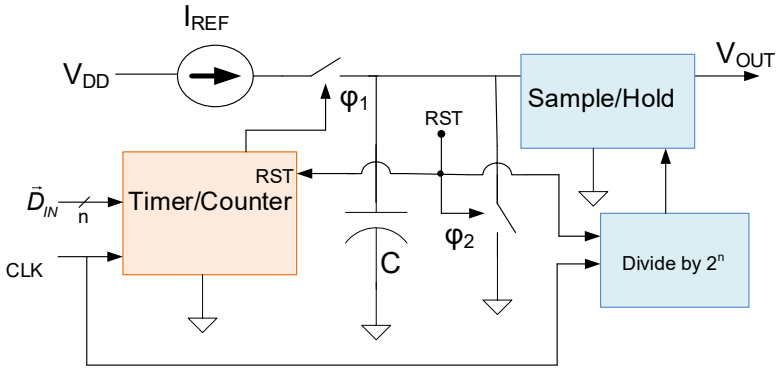
Sample/Hold can sample output just before reset and hold for 2^n clock transitions

Is this an MDAC? Yes – but multiplying factor is I_{REF}

Can it be a 2-quadrant or 4-quadrant MDAC? Yes

DAC Architectures

Single Slope



Single-Slope DAC

Can be viewed as a time-domain DAC where resolution headroom is very large

Benefits of Single-Slope ADC?

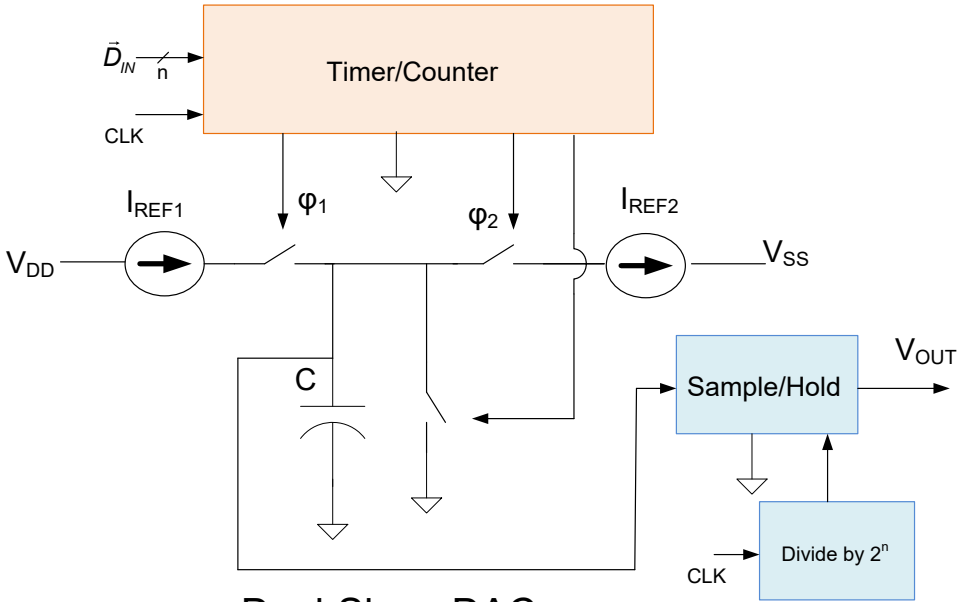
- No matching required
- Very simple structure
- Mostly Digital
- Very low DNL
- Very fine resolution possible
- No previous code dependence
- No binary to thermometer decoder

Limitations of Single-Slope ADC?

- Slow conversion rate
- Large C
- Leakage currents that will be temperature dependent
- Nonlinearity in C?
- Nonlinearity in I_{REF}

DAC Architectures

Dual Slope



Dual-Slope DAC

Provides DAC with positive and negative outputs

Term “dual slope” means something different here than what we see in “dual slope” ADCs

Is this an MDAC? Yes if $I_{REF1}=I_{REF2}=I_{REF}$ but multiplying factor is I_{REF}

What DAC Architectures are Actually Used?

Listing from Texas Instruments March 1 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

DAC8532 Dual Channel, 16-Bit, Low Power, Serial Input Digital-To-Analog Converter

1 Features

- 16-Bit Monotonic Over Temperature
- *Micro*Power Operation: 500 µA at 5 V
- Power-On Reset to Zero-Scale
- Power Supply: 2.7 V to 5.5 V
- Settling Time: 10 µs to ±0.003% FSR
- Ultra-Low AC Crosstalk: –100 dB Typ
- Low-Power Serial Interface With Schmitt-Triggered Inputs
- On-Chip Output Buffer Amplifier With Rail-to-Rail Operation
- Double-Buffered Input Architecture
- Simultaneous or Sequential Output Update and Powerdown
- Available in a Tiny VSSOP-8 Package

2 Applications

- Portable Instrumentation
- Closed-Loop Servo Control
- Process Control
- Data Acquisition Systems
- Programmable Attenuation
- PC Peripherals

3 Description

The DAC8532 is a dual channel, 16-bit digital-to-analog converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7 V to 5.5 V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30 MHz for V_{DD} = 5 V.

The DAC8532 requires an external reference voltage to set the output range of each DAC channel. The device incorporates a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8532 provides a flexible power-down feature, accessible over the serial interface, that reduces the current consumption of the device to 200 nA at 5 V.

The low-power consumption of the device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 2.5 mW at 5 V, reducing to 1 µW in power-down mode.

The DAC8532 is available in a VSSOP-8 package with a specified operating temperature range of –40°C to 105°C.

Device Information[1]

7.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative accuracy				±0.0987	% of FSR
Differential nonlinearity	16-bit monotonic			±1	LSB
Zero code error			5	25	mV
Full-scale error			–0.15	–1	% of FSR
Gain error				±1	% of FSR
Zero code error drift			±20		µV/°C
Gain temperature coefficient			±5		ppm of FSR/°C
Channel-to-channel matching PSRR	R_L = 2 kΩ, C_L = 200 pF		15		mV
			0.75		mV/V

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

Ironically INL not specified in datasheet but listed as 64 LSB in selection guide

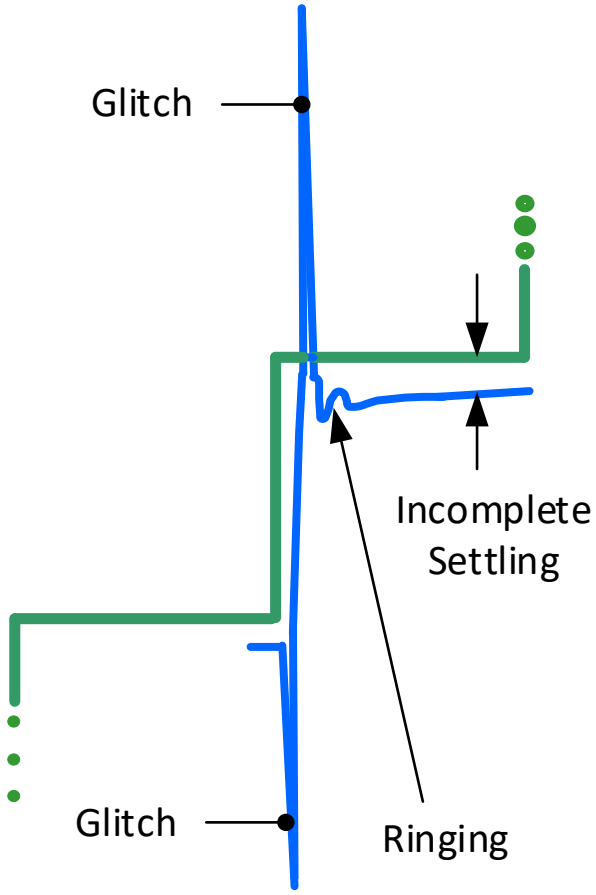
16-bit TI String DACs

				INL
DAC8775	16	$15.880 | 1ku	String	12
DAC8551-Q1	16	$2.950 | 1ku	String	16
DAC8563T	16	$4.066 | 1ku	String	12
DAC8562T	16	$4.066 | 1ku	String	12
DAC8563-Q1	16	$4.798 | 1ku	String	12
DAC8750	16	$4.970 | 1ku	String	26
DAC8760	16	$5.900 | 1ku	String	52
DAC8562-Q1	16	$4.798 | 1ku	String	12
DAC8562	16	$4.066 | 1ku	String	12
DAC8563	16	$3.860 | 1ku	String	12
DAC8718	16	$23.990 | 1ku	String	4
DAC8728	16	$23.990 | 1ku	String	4
DAC8568	16	$10.600 | 1ku	String	12
DAC8411	16	$2.420 | 1ku	String	8
DAC8564	16	$6.282 | 1ku	String	8
DAC8565	16	$6.785 | 1ku	String	8
DAC8560	16	$2.890 | 1ku	String	8
DAC8552	16	$3.800 | 1ku	String	12
DAC8550	16	$3.000 | 1ku	String	8
DAC8555	16	$6.070 | 1ku	String	12
DAC8554	16	$6.490 | 1ku	String	12
DAC8551	16	$2.500 | 1ku	String	12
DAC8544	16	$13.000 | 1ku	String	65
DAC8571	16	$2.420 | 1ku	String	65
DAC8574	16	$7.647 | 1ku	String	64
DAC8534	16	$9.605 | 1ku	String	64
DAC8532	16	$5.785 | 1ku	String	65
DAC8541	16	$2.904 | 1ku	String	65
DAC8501	16	$3.263 | 1ku	String	64
DAC8531	16	$3.245 | 1ku	String	64

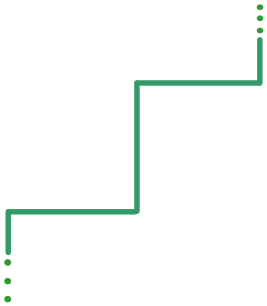
>16-bit TI R-2R DACs

				INL
DAC11001B	20	$59.000 | 1ku	R-2R	1
DAC11001A	20	$35.778 | 1ku	R-2R	4
DAC91001	18	$27.489 | 1ku	R-2R	1
DAC9881	18	$16.359 | 1ku	R-2R	2
DAC82002	16	$14.000 | 1ku	R-2R	2
DAC81402	16	$8.900 | 1ku	R-2R	1
DAC81404	16	$15.990 | 1ku	R-2R	1
DAC81001	16	$17.589 | 1ku	R-2R	1
DAC80502	16	$3.949 | 1ku	R-2R	1
DAC80501	16	$2.750 | 1ku	R-2R	1
DAC81408	16	$23.990 | 1ku	R-2R	1
DAC81416	16	$32.990 | 1ku	R-2R	1
DAC80504	16	$8.702 | 1ku	R-2R	1
DAC80508	16	$9.240 | 1ku	R-2R	1
DAC80004	16	$7.734 | 1ku	R-2R	1
DAC161S055	16	$4.840 | 1ku	R-2R	3
DAC8734	16	$19.990 | 1ku	R-2R	1
DAC8881	16	$8.906 | 1ku	R-2R	1
DAC8871	16	$25.000 | 1ku	R-2R	1
DAC8831-EP	16	$12.013 | 1ku	R-2R	1
DAC8830-EP	16	$11.664 | 1ku	R-2R	1
DAC8832	16	$5.760 | 1ku	R-2R	1
DAC8831	16	$6.242 | 1ku	R-2R	1
DAC8830	16	$5.910 | 1ku	R-2R	1
DAC7664	16	$26.378 | 1ku	R-2R	3
DAC7654	16	$38.165 | 1ku	R-2R	3
DAC7742	16	$13.665 | 1ku	R-2R	3
DAC7632	16	$10.116 | 1ku	R-2R	3
DAC7642	16	$14.741 | 1ku	R-2R	3
DAC7741	16	$9.244 | 1ku	R-2R	3
DAC7731	16	$8.335 | 1ku	R-2R	3
DAC7631	16	$7.209 | 1ku	R-2R	3
DAC7641	16	$8.334 | 1ku	R-2R	3
DAC7734	16	$37.464 | 1ku	R-2R	2
DAC7634	16	$24.576 | 1ku	R-2R	3
DAC7744	16	$38.643 | 1ku	R-2R	2
DAC7644	16	$21.282 | 1ku	R-2R	3
DAC716	16	$23.642 | 1ku	R-2R	2
DAC715	16	$25.556 | 1ku	R-2R	2
DAC714	16	$20.350 | 1ku	R-2R	1

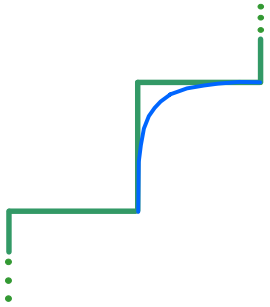
DAC Performance Issues and Concerns



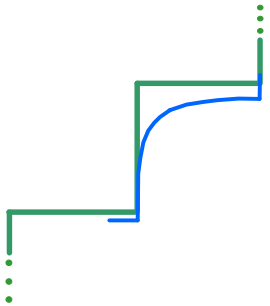
DAC Performance Issues and Concerns



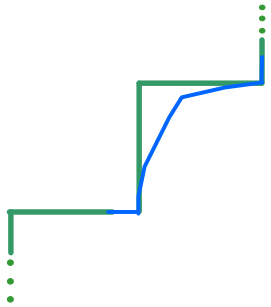
Ideal



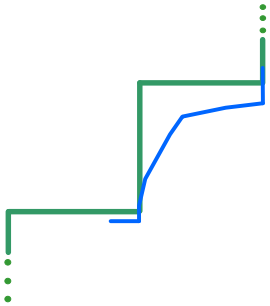
Complete
Linear Settling



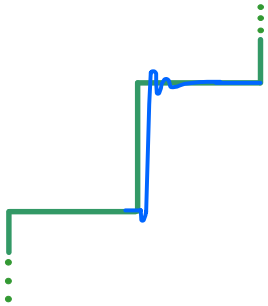
Incomplete
Linear Settling



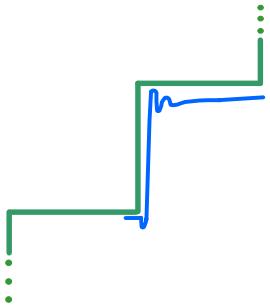
Complete Nonlinear
Settling



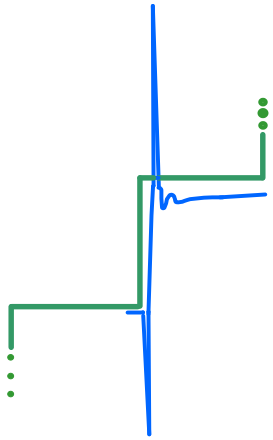
Incomplete
Nonlinear Settling



Complete with glitch

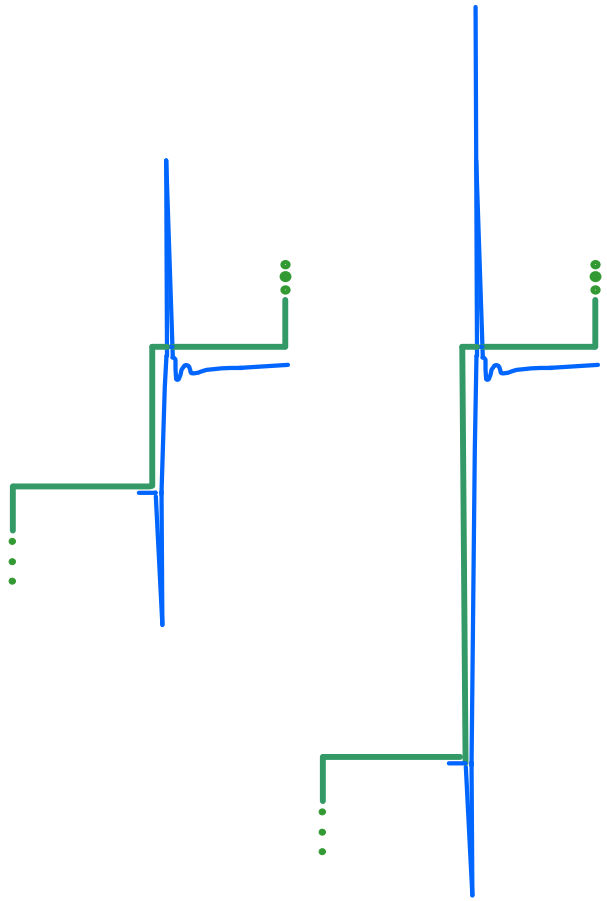


Incomplete with
glitch

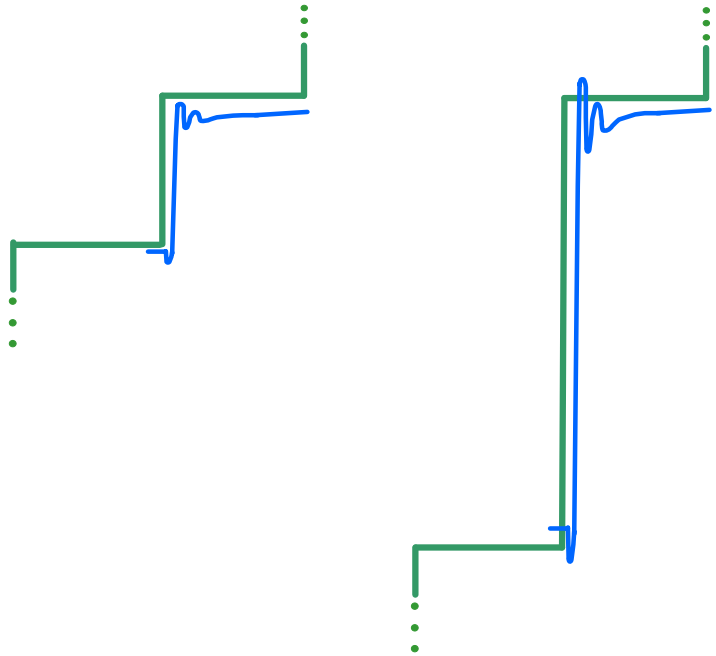


Incomplete with big
glitch

DAC Performance Issues and Concerns



Previous code dependent glitches



Previous code dependent settling

DAC Performance Issues and Concerns

Linear settling of DAC outputs do not affect linearity if all have same settling times (for both sampled outputs and overall transient response

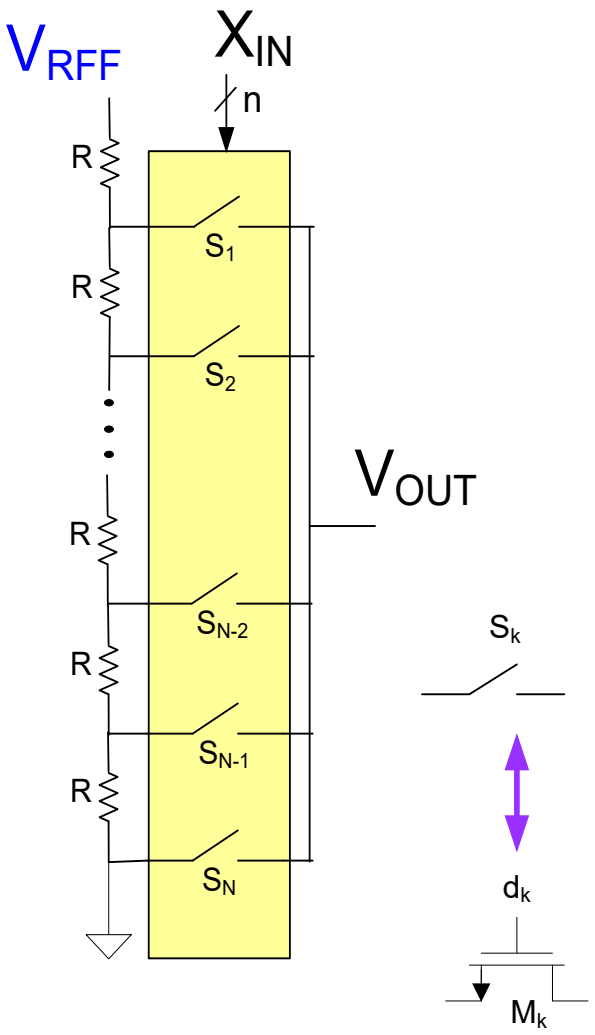
Incomplete settling introduces nonlinearities in transient response and usually in settled response

Previous code dependent outputs or settling almost always introduces nonlinearities

Glitches can be many LSB in magnitude and are often previous-code dependent

Glitches in output at transition points do not introduce nonlinearities in settled outputs but may introduce distortion in continuous-time outputs

R-String DAC



Conceptual

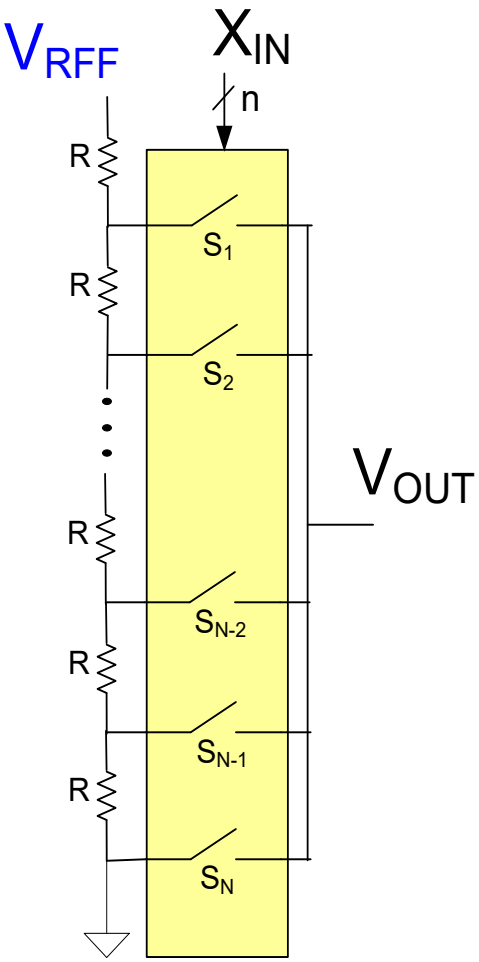
- ❑ Simple structure
- ❑ Inherently monotone
- ❑ Very low DNL
- ❑ Potential for being very fast
- ❑ Low Power Dissipation
- ❑ Widely Used Approach (with appropriate considerations)

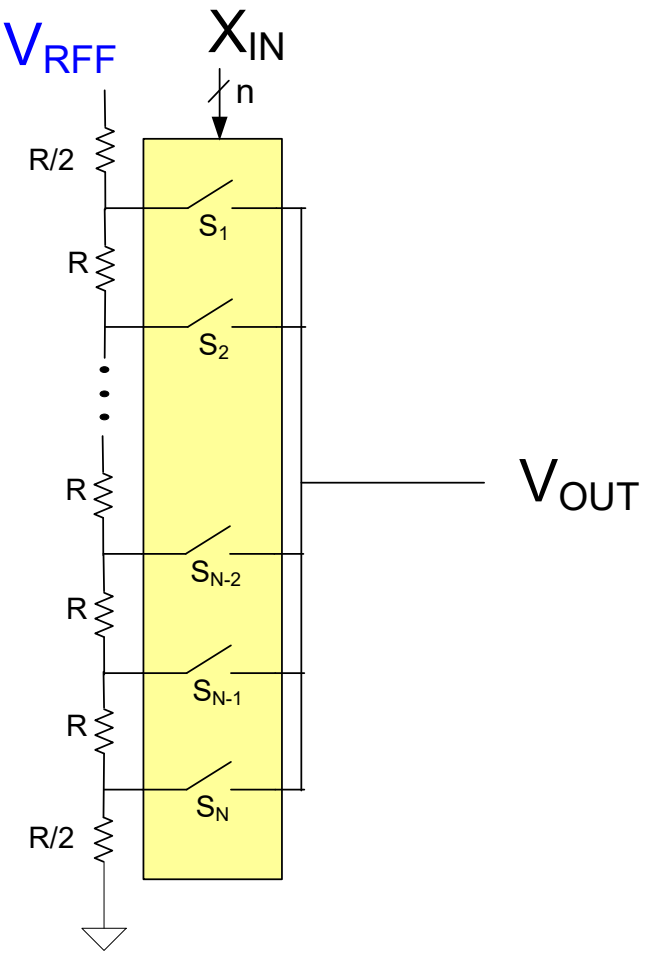
Challenges:

- Managing INL
- Matching (resistors, switches)
- Leakage currents
- Large number of devices for n large (2^n or 2^{n+1} lines)
- Decoder
- Routing thermometer/bubble clocks
- Transients during Boolean transitions
- Glitches
- Switch implementation
- Thevenin impedance facing V_{OUT} highly code dependent

R-String DAC

(minor variant where $V_{OUT}(0,\ldots 0) \neq 0$)



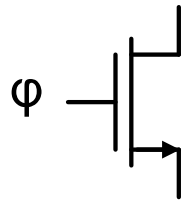


Practical level shift

Switch Implementation

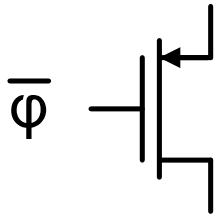
Basic Switch

- Large number required for large resolution
- Simple structure often used



single n-channel device

- Good when switch terminals near gnd
- Will not turn on when terminals near V_{DD}



single p-channel device

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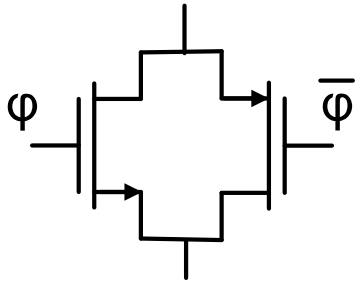
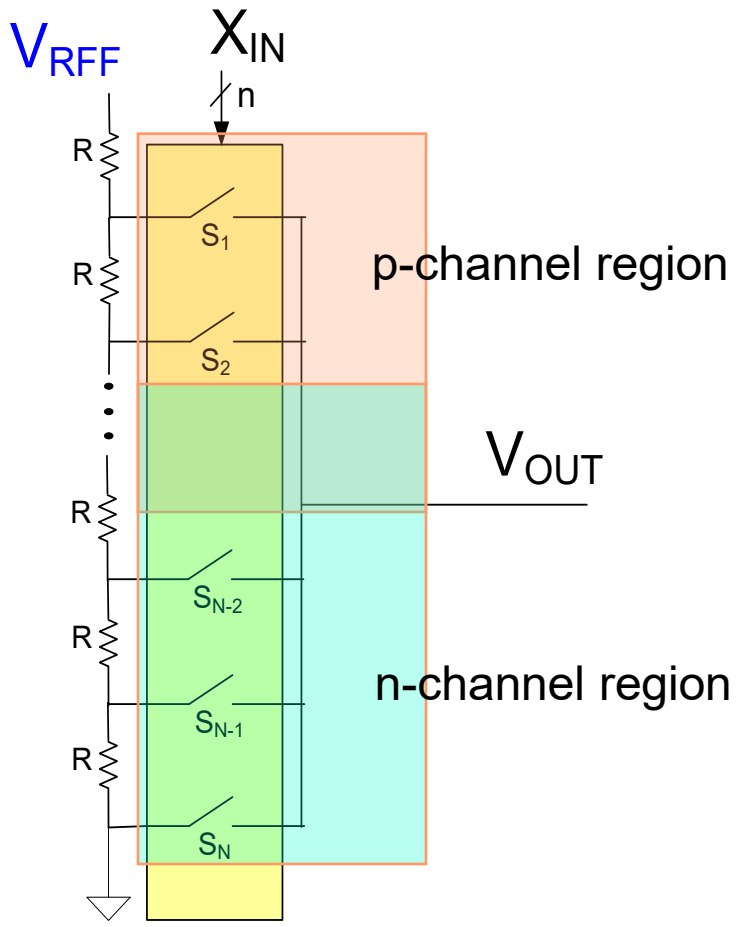


transmission gate switch

- Use devices where cross-over occurs
- Good for both high and low term voltages
- Extra clock signal required
- Try to avoid this complexity

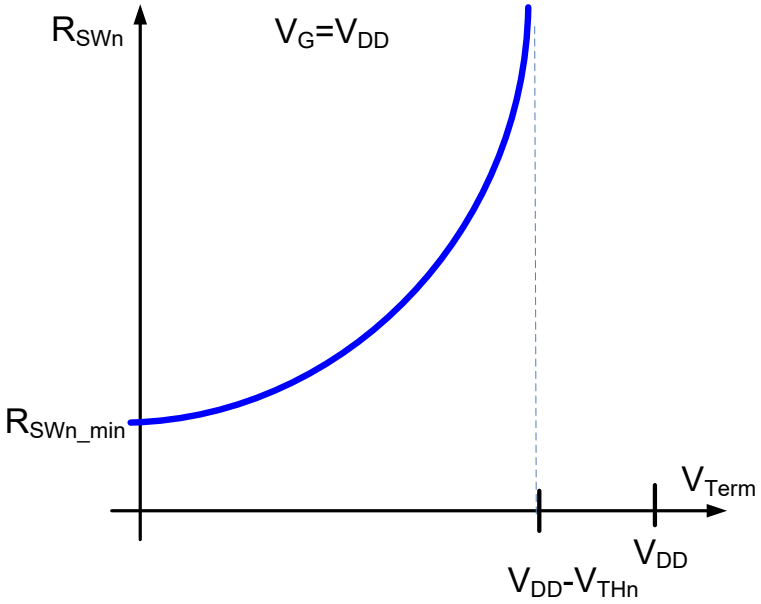
Other switch structures (such as bootstrapped switch) used but not for basic string DACs

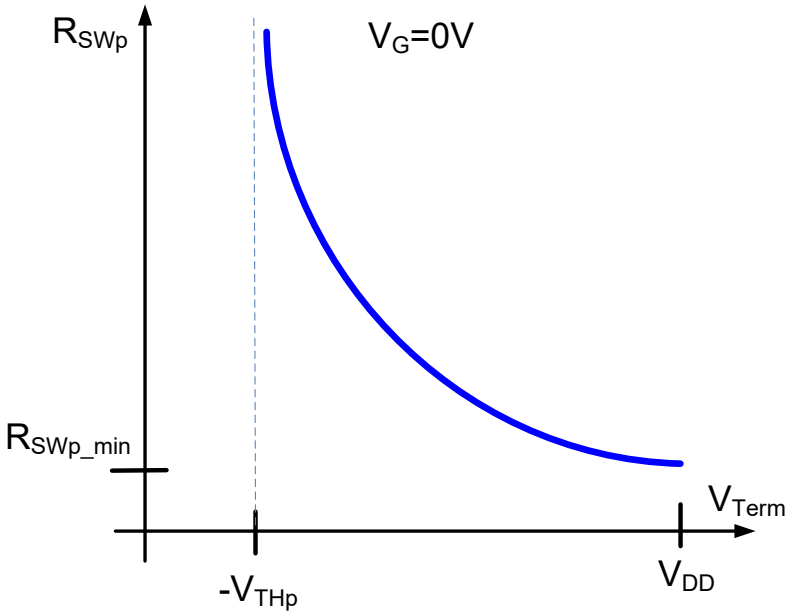
Switch Assignment

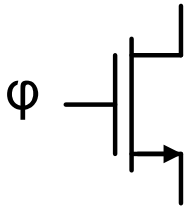


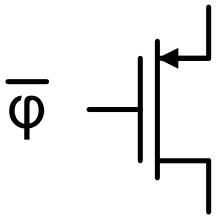
Challenges:

Switch Impedances

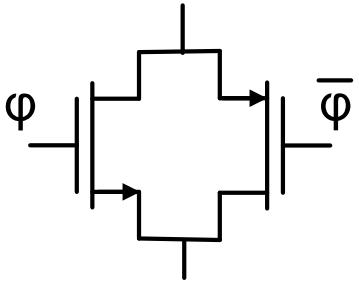


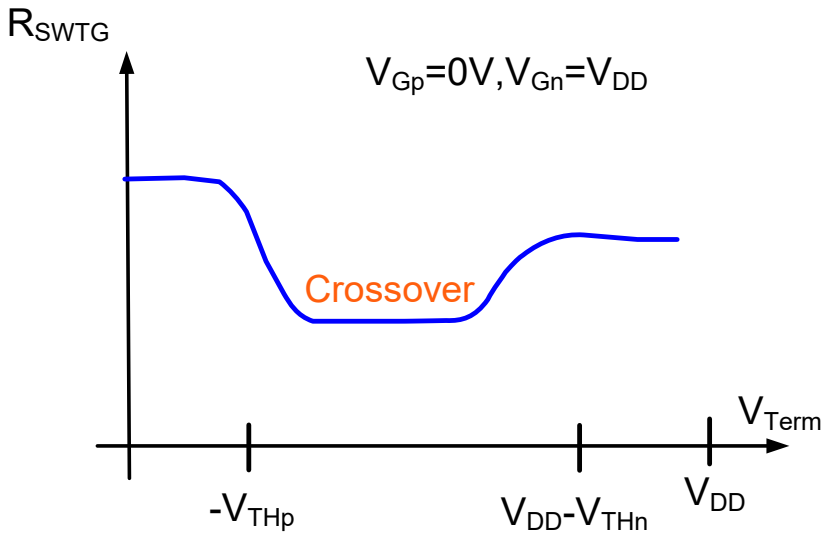


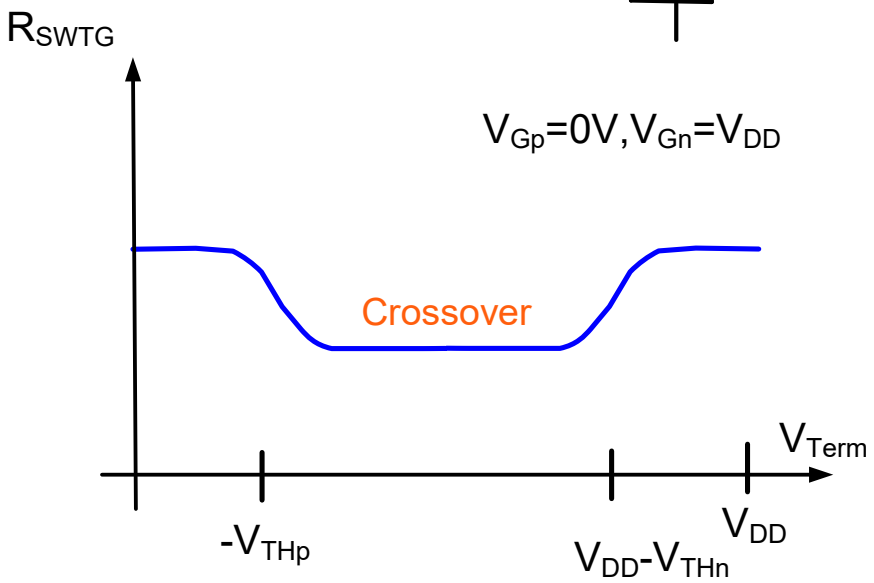


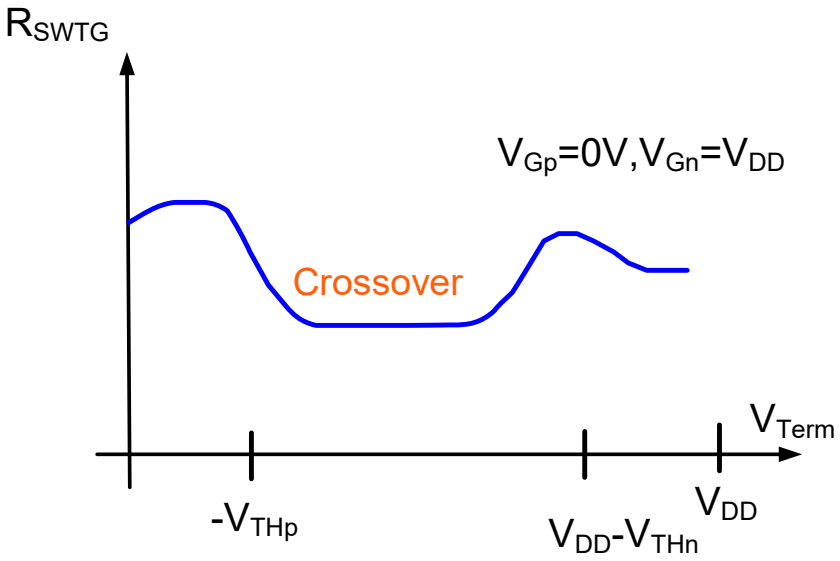


Switch Impedances



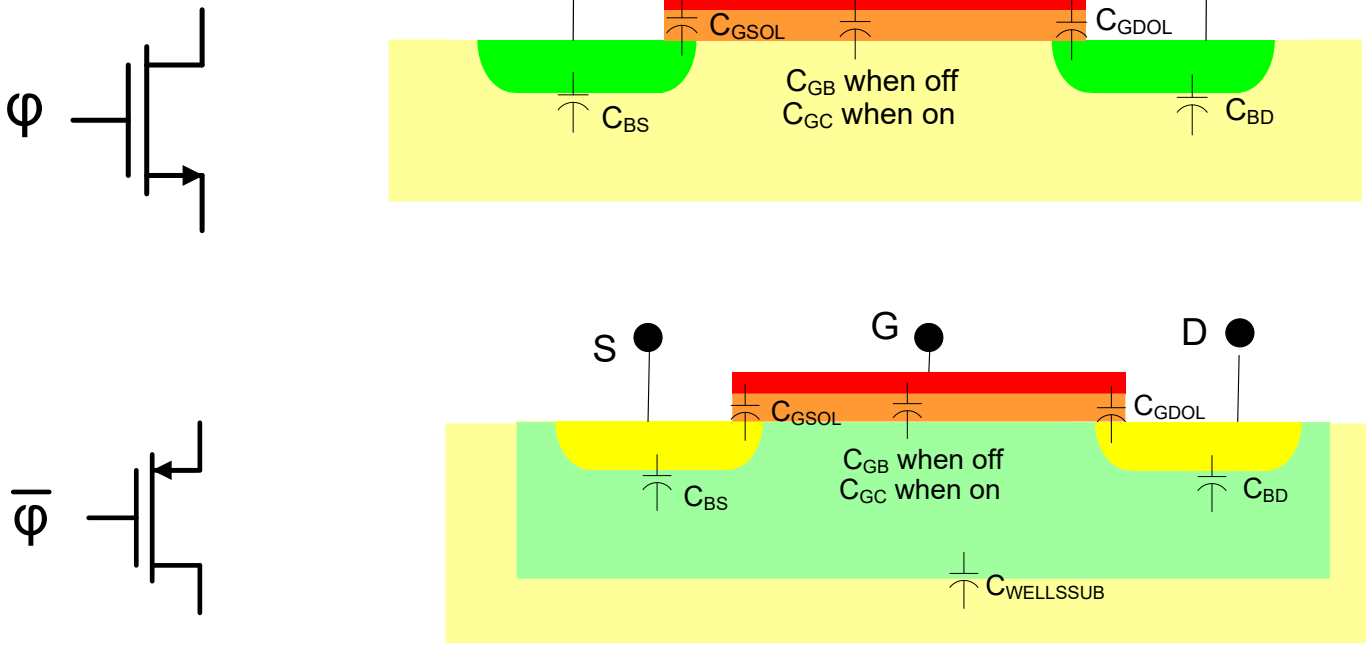






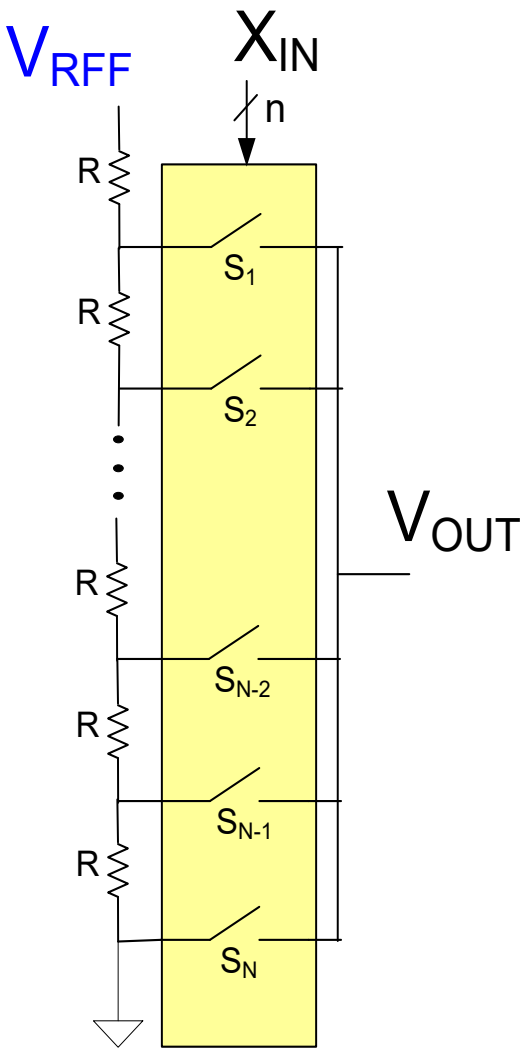
Switch impedance significantly both position and device size dependent

Switch Parasitics



- C_{BD} and C_{BS} can be significant and cause rise-fall times to be position dependent
- C_{GDOL} can cause “kickback” or feed-forward
- C_{GS} can slow turn-on and turn-off time of switch

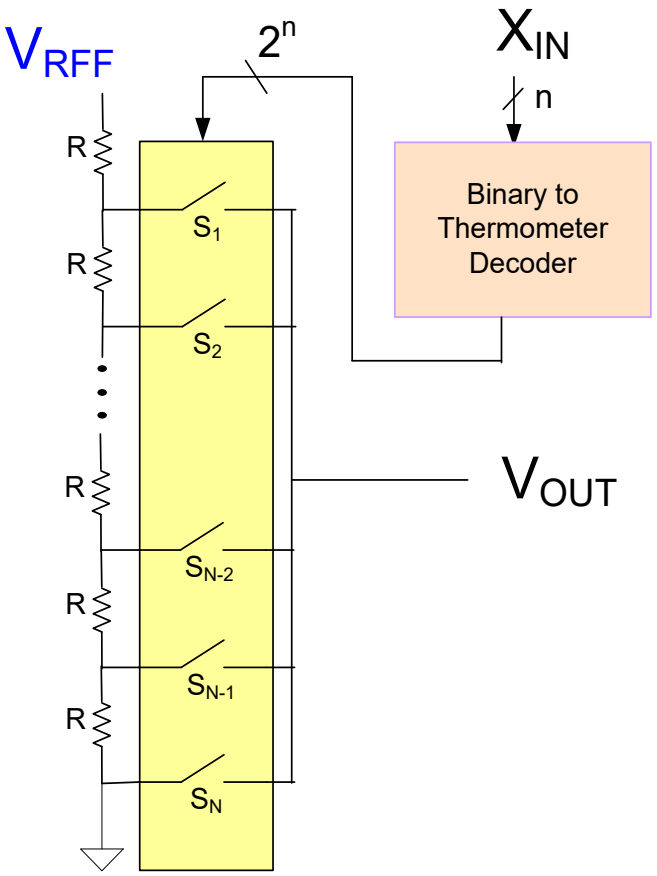
R-String DAC



Additional Challenges:

- Capacitance on V_{OUT} can be large
  - larger for p-channel devices
  - even larger for TG switches
- Switch impedances position dependent
- Kickback from switches to R-string
- Capacitance on each node (though small) of R-string from switch
- Thevenin impedance facing V_{OUT} highly code dependent
- Gradient effects may cause nonlinearities since common-centroid layout may not be practical if n is large

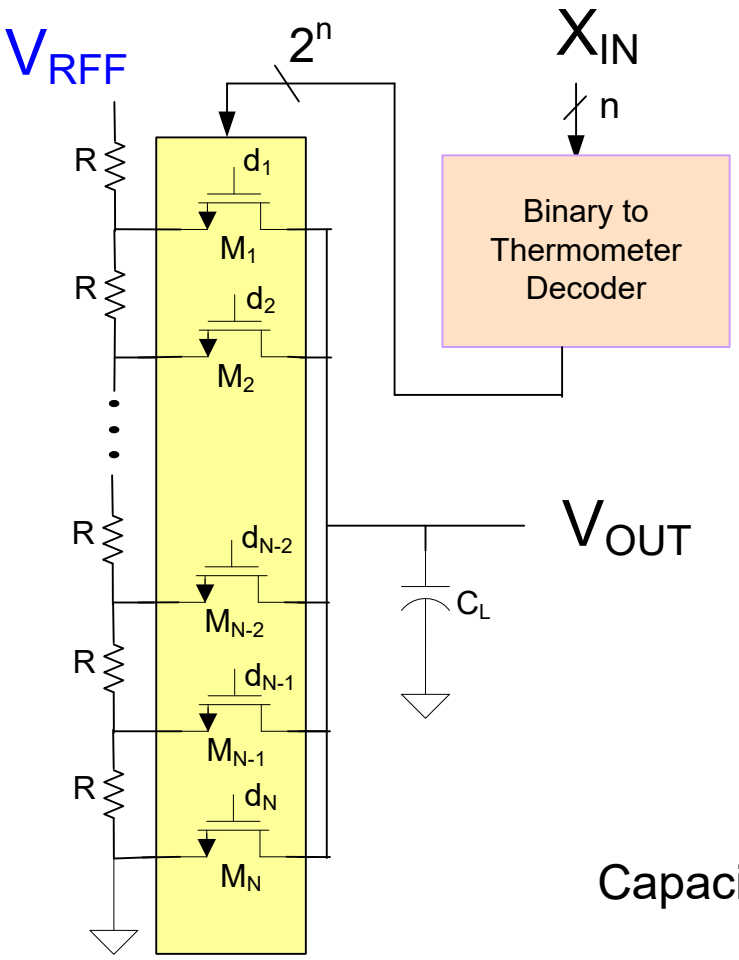
R-String DAC



Additional Challenges

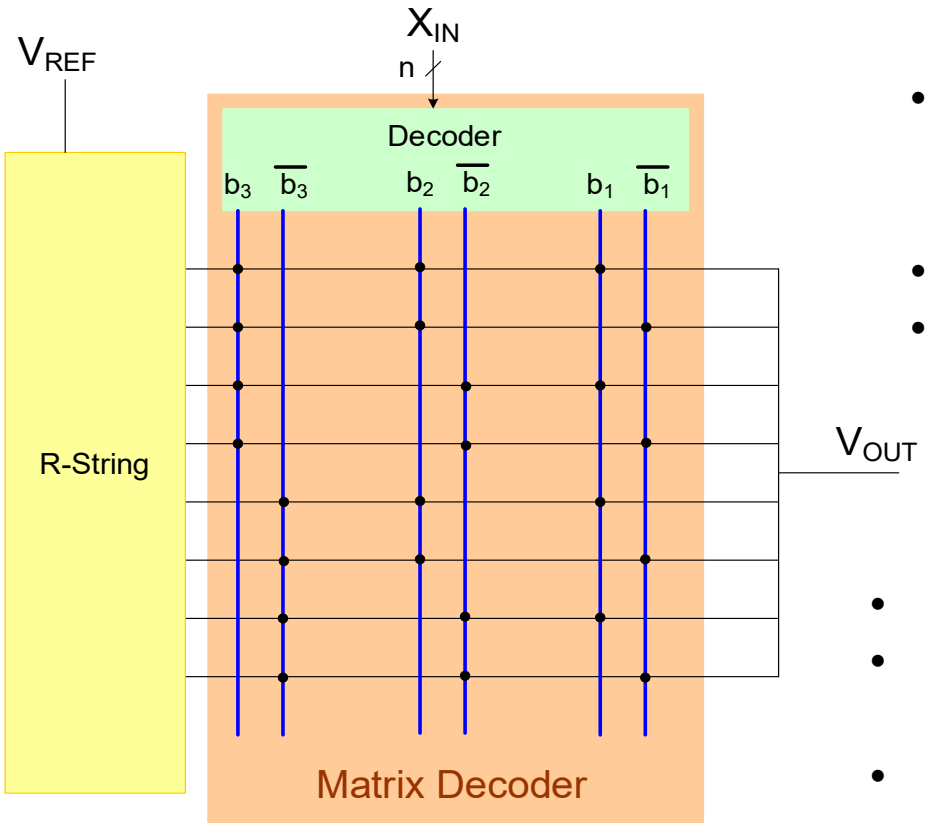
- Delay in Decoder may be significant
- Delay in Decoder may be previous code and current code dependent
- Intermediate undesired Boolean outputs may occur
  - These may cause undesired opening and closing of switches
  - Could momentarily short out taps on R-string
  - Could introduce transients on all nodes of R-string that are code and previous code dependent

R-String DAC



Capacitive loading due to switches

R-String DAC

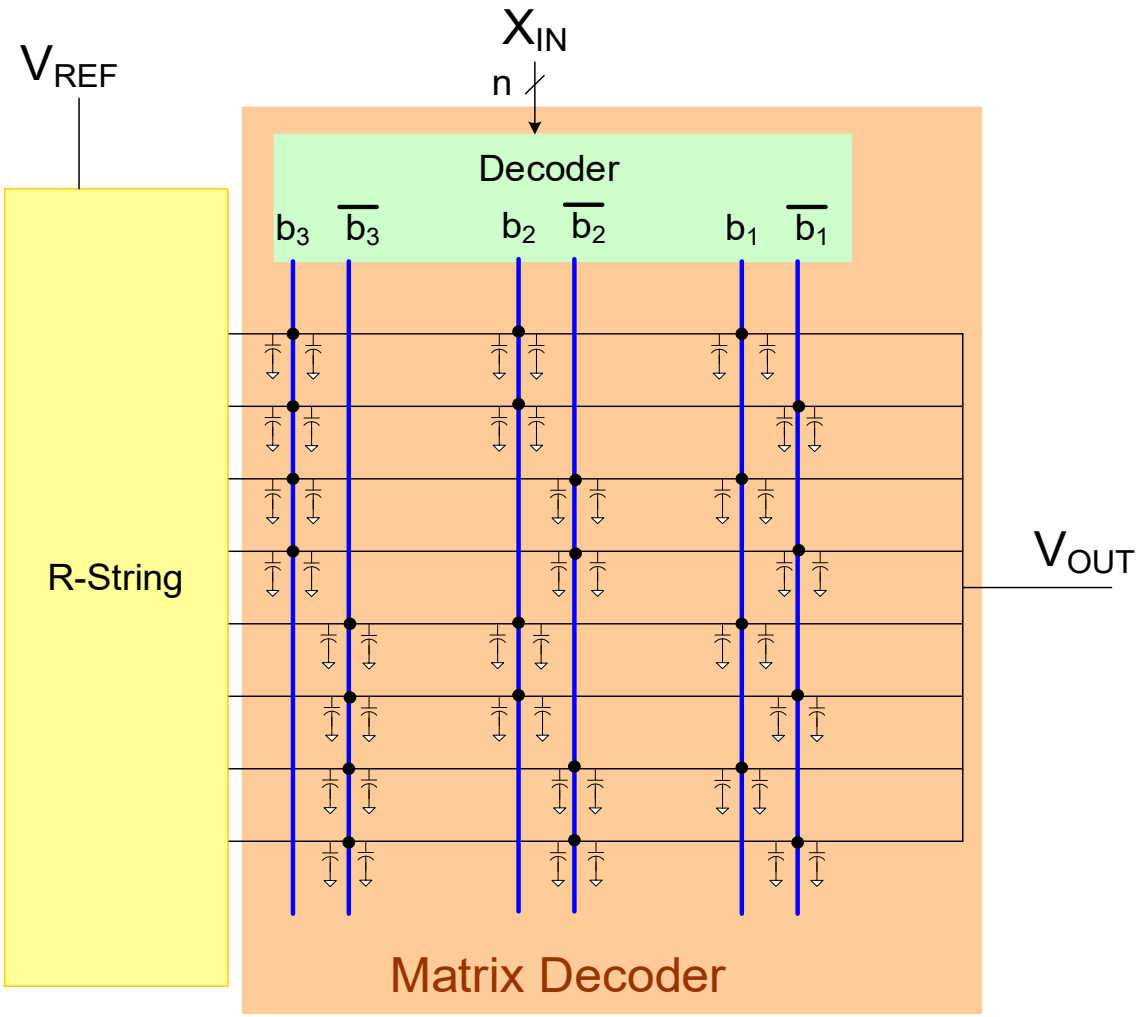


- Uses matrix decoder as analog MUX (don't synthesize decoder)
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)

Challenges

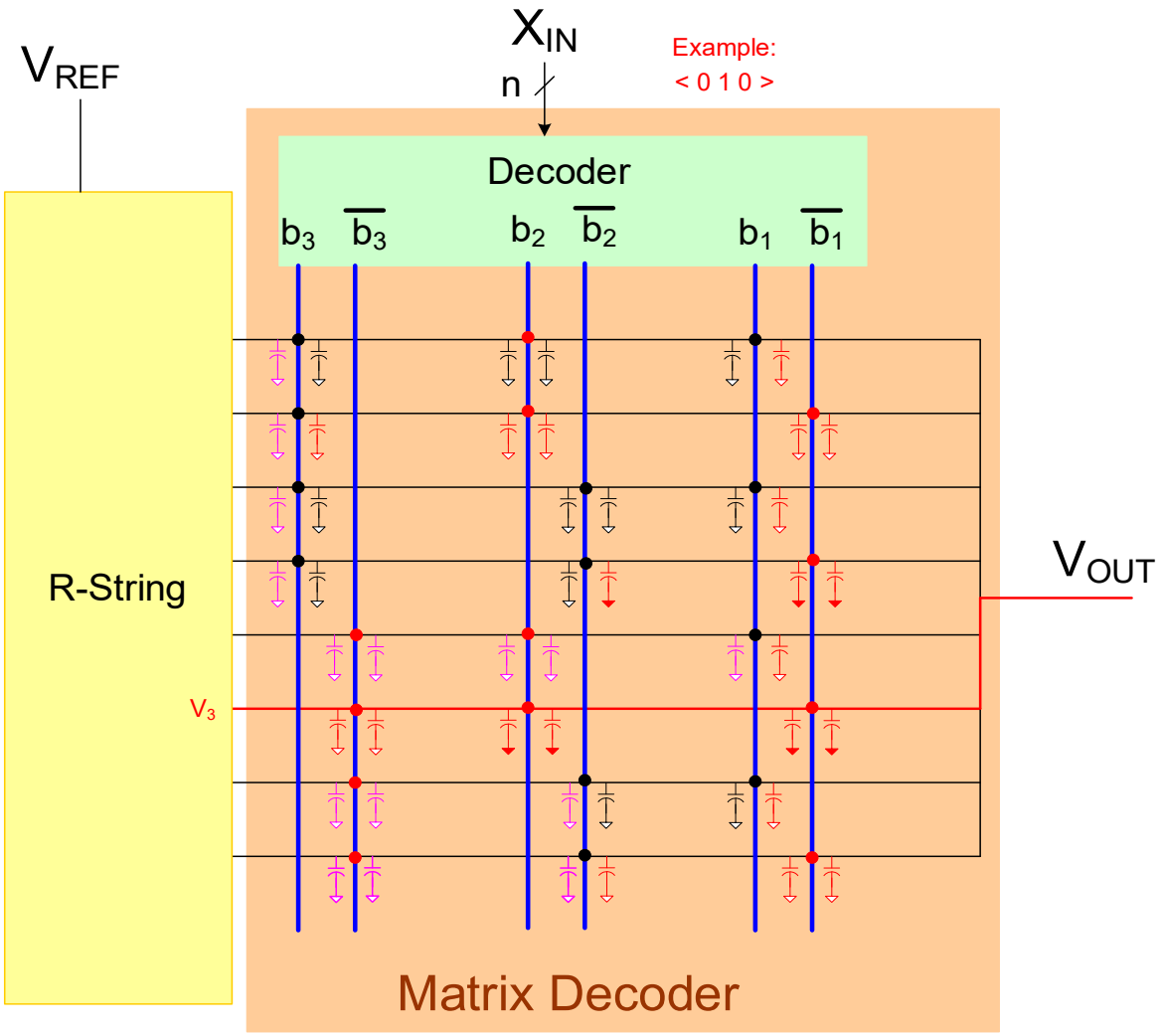
- Still many signals to route
- Large capacitance on V_{OUT} (over 2^{n+1} diff caps)
- Multiple previous code dependencies cause output transition time to be quite unpredictable
- Considerable transients introduced on R-string

R-String DAC



Parasitic Capacitances in Matrix Decoder

R-String DAC



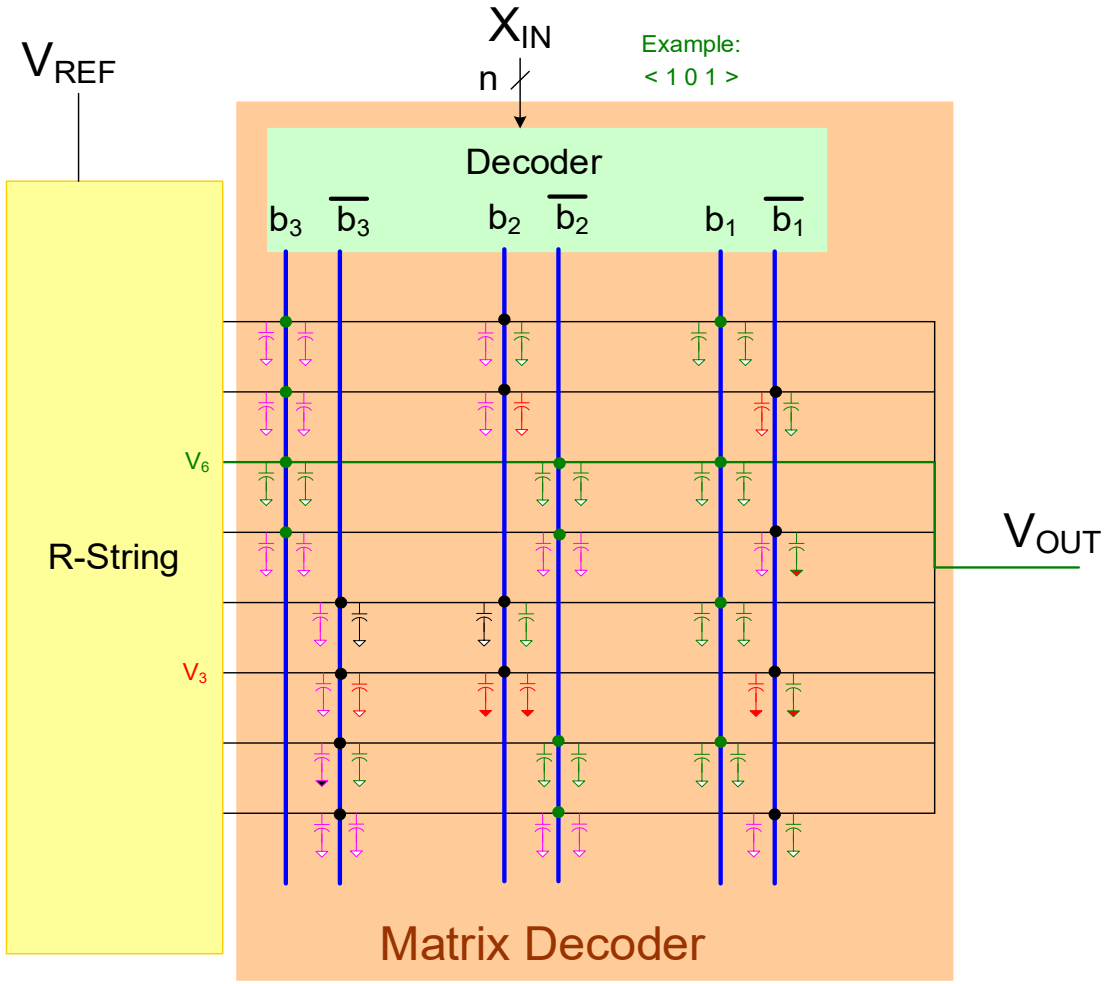
Previous-Code Dependent Settling

Assume all C's (except those on the R-string) initially with 0V

Red denotes V_3, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>



Previous-Code Dependent Settling

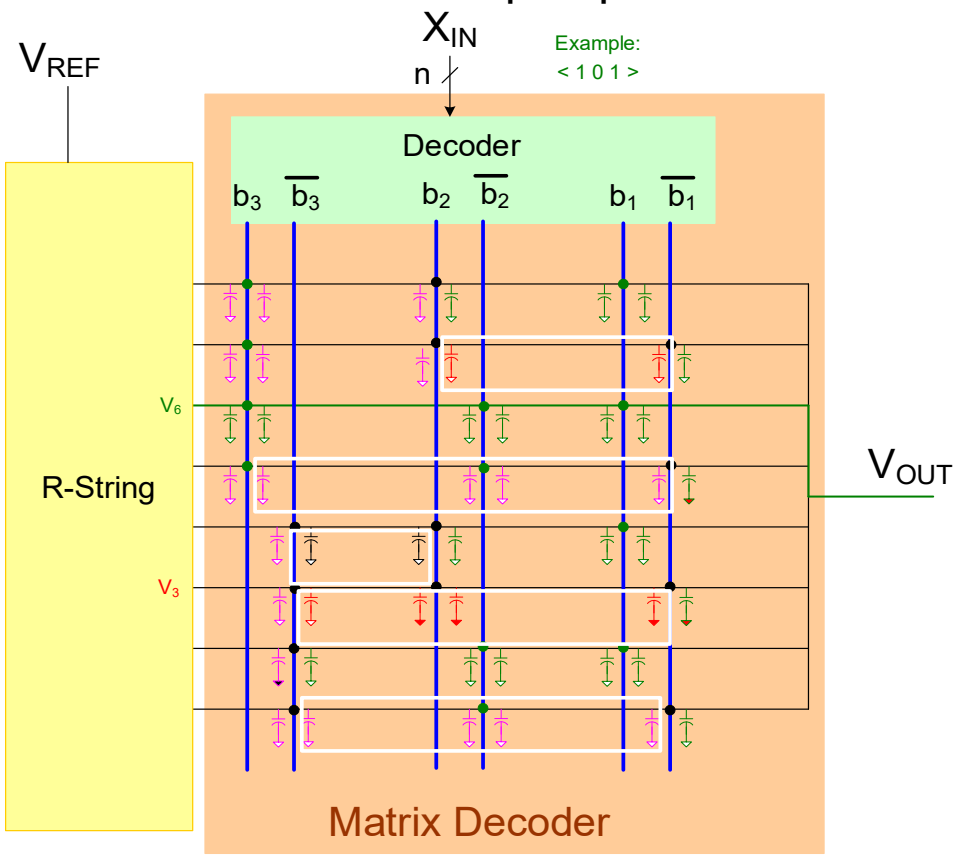
Assume all C's (except those on the R-string) were initially at 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>

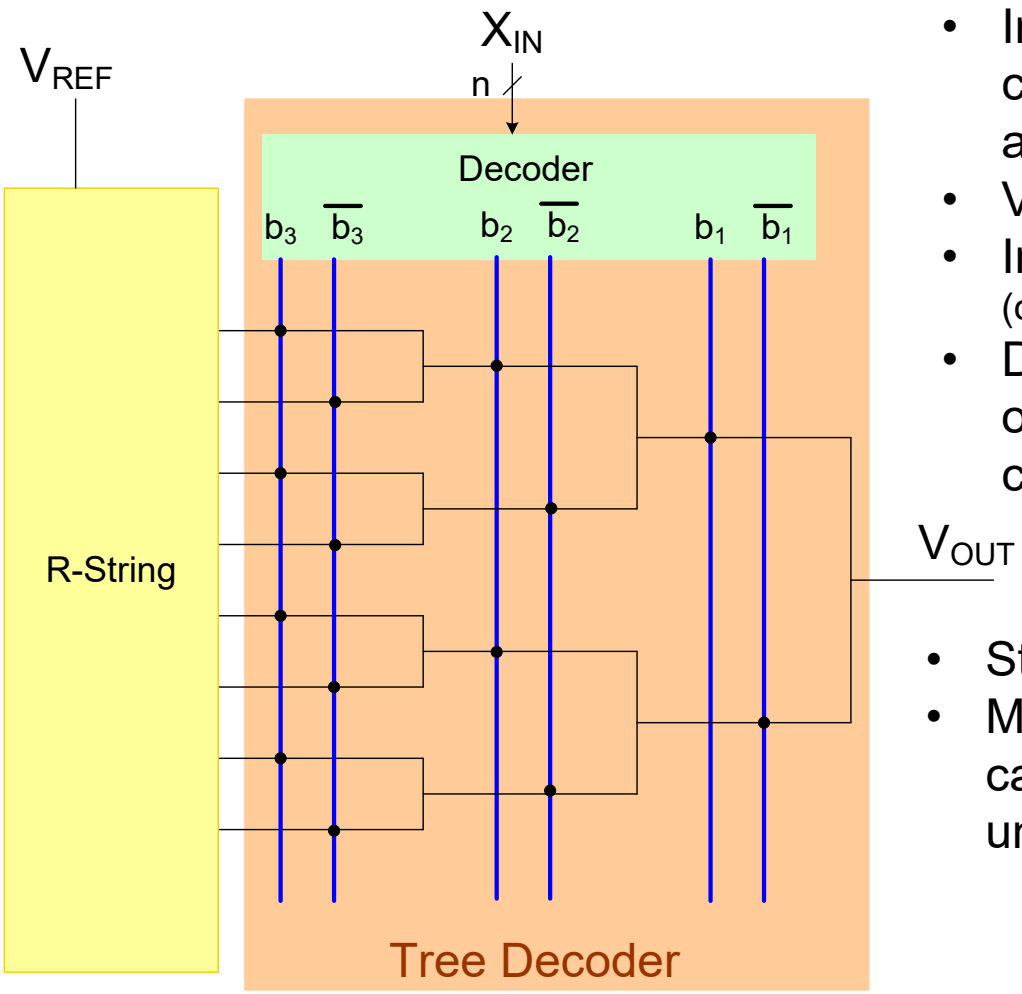
White boxes show capacitors dependent upon previous code <010>



Previous-Code Dependent Settling

- Assume all C's (except those on the R-string) were initially at 0V
- Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage
- Some capacitors may retain values from a previous input for many clock cycles for some inputs resulting in previous-previous dependence of even longer

R-String DAC

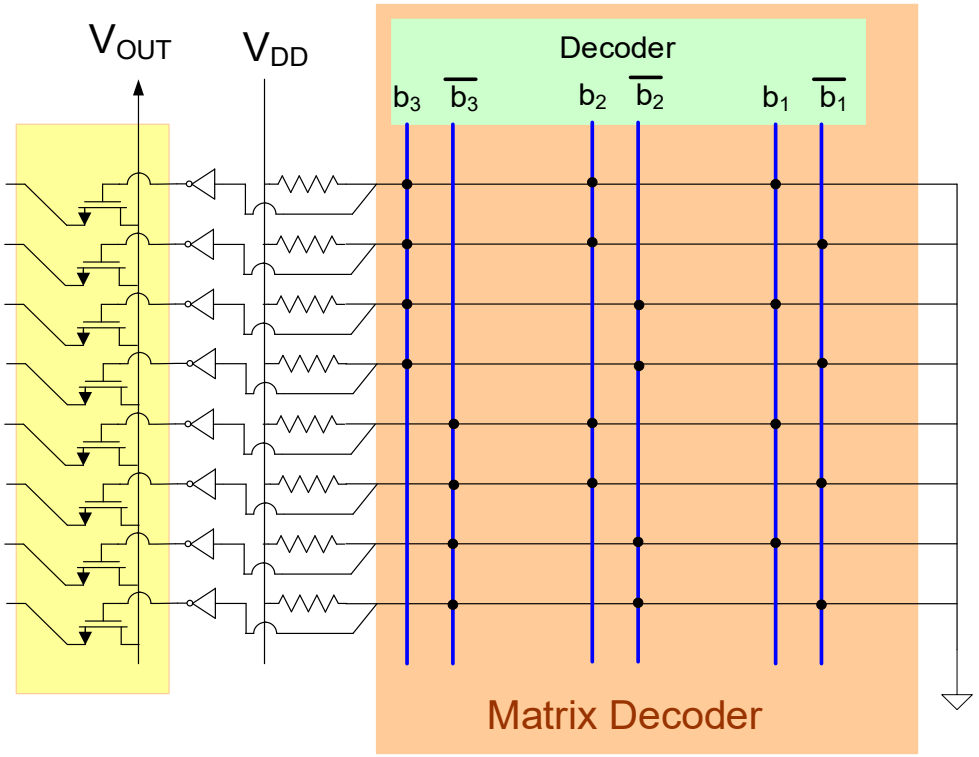


- Uses tree decoder as analog MUX
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)
- Dramatically reduces capacitance on output and switching capacitances

Challenges

- Still many signals to route
- Multiple previous code dependencies cause output transition time to be quite unpredictable

R-String DAC



Matrix-Decoder in Digital Domain

Single transistor used at each marked intersection for PTL AND gates

Significant reduction in capacitive loading at output

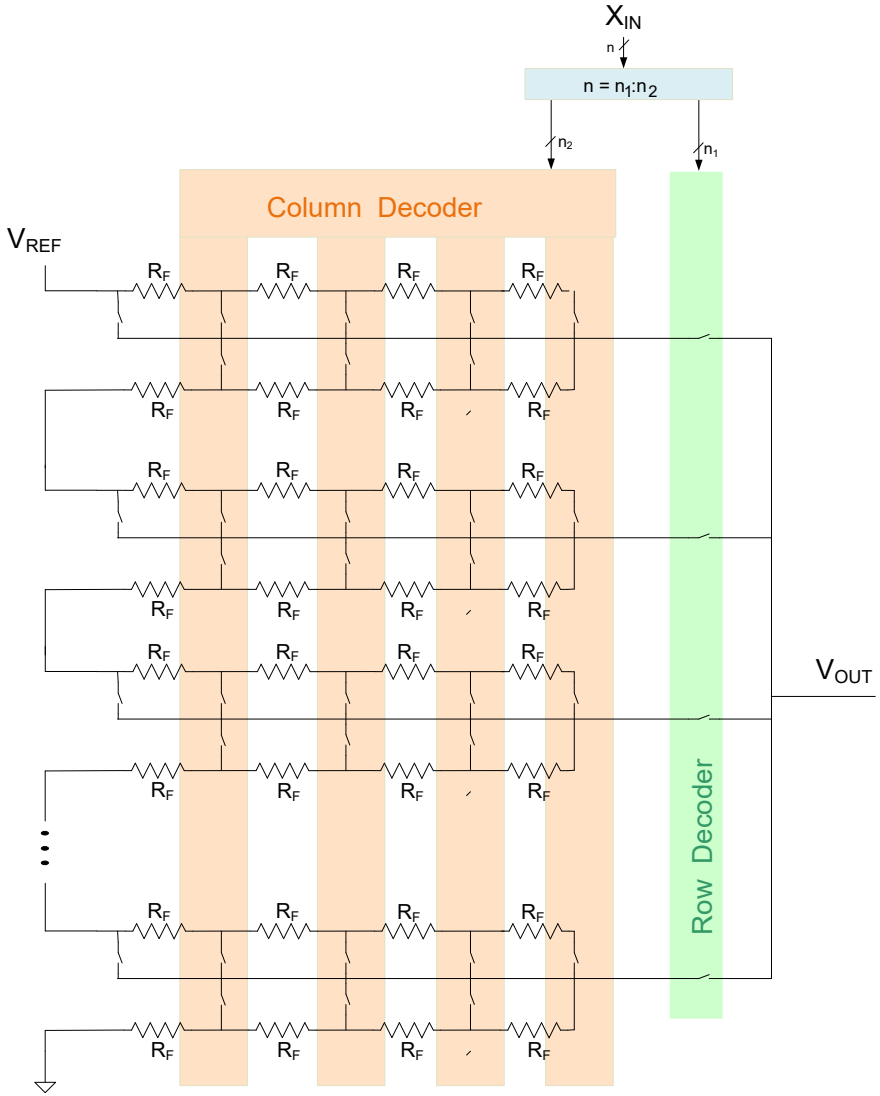
Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

Will become more complicated if both p-channel and n-channel switches needed

R-String DAC

String DAC with Row-Column Decoder

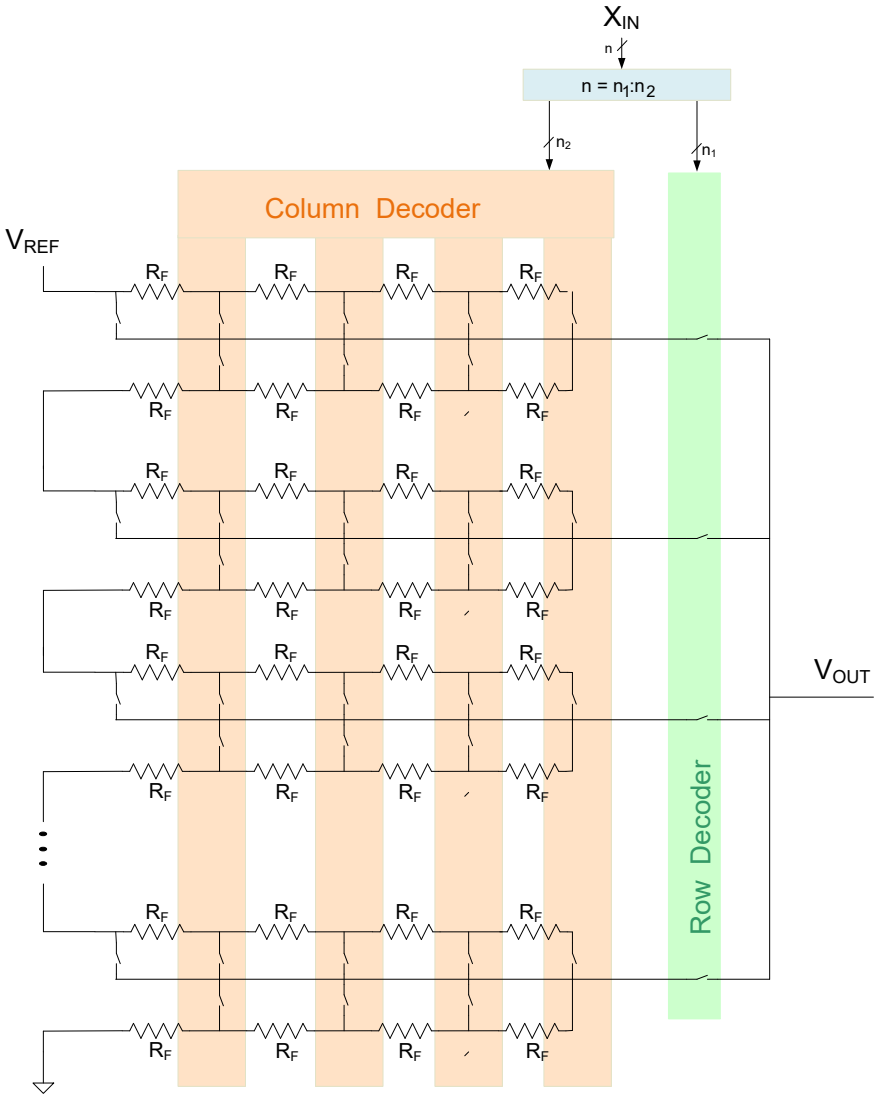


- Dramatic reduction in decoder complexity
- Dramatic reduction of capacitive loading on output
- Changes decoder from a one-dimensional to a two-dimensional solution (can be thought of as folding)
- Logic gates could be placed at each node to eliminate analog row decoder

Challenges (most were present in earlier structures too)

- Some previous code dependence
- INL large
- Difficult to cancel gradient effects in layout
  - Switching sequencing can help a lot
- Switch impedances code dependent
- Settling times code dependent

R-String DAC

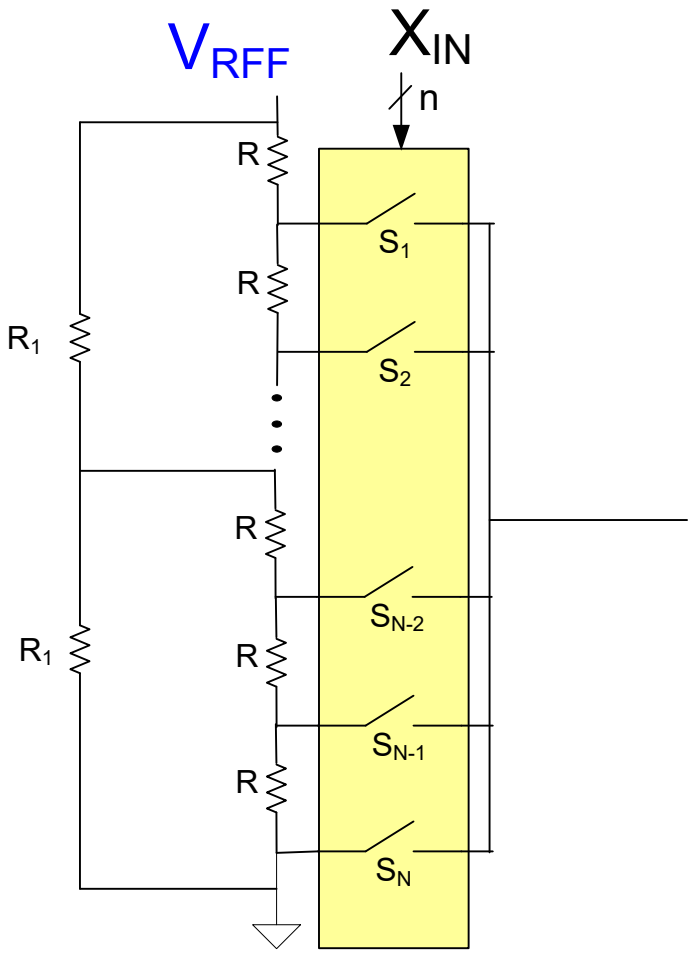


Can this concept be extended further?

- Dramatic reduction in decoder complexity
- Dramatic reduction of capacitive loading on output
- Changes decoder from a one-dimensional to a m-dimensional solution (folding)
- Logic gates could be placed at each node to eliminate analog row decoder

R-String DAC

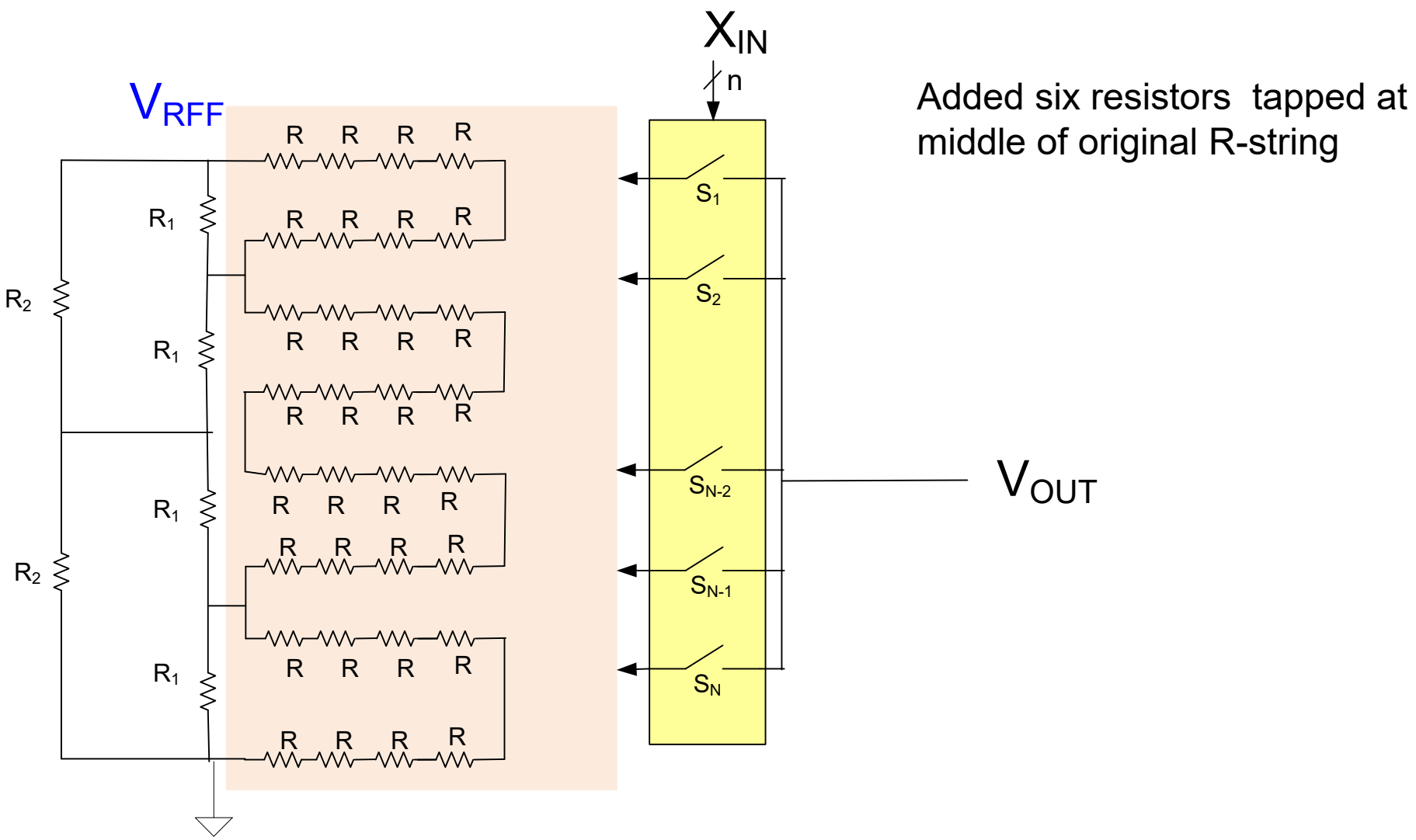
What about this parallel R-string?



Added two resistors tapped at middle of original R-string

R-String DAC

What about this parallel R-string?



Added six resistors tapped at middle of original R-string

Stay Safe and Stay Healthy !

End of Lecture 13